

RIC

DATA SHEET**Reset/Interrupt/Clock Controller**

DESCRIPTION

The STP2210QFP (RIC⁽¹⁾) supports the system resets, system interrupts, system scan, and system clock-control functions. These are independent blocks, designed onto the ASIC chip to save space and improve reliability. Note that there are no major data paths between these blocks.

FEATURES

- Supports resets from power supply, reset buttons, and scan. Generates and delivers resets to the System Controller (SC).
- Concentrates all the interrupts and sends interrupt codes to the U2S (UPA-to-SBus Interface)
- Directs Scan inputs and outputs through scan chains
- Determines the system speed from CPU speed inputs
- Provides decoding for the:
 - System Controller (SC)
 - Lab Console address and data registers
 - Frequency margining chip
 - PROM write address space

1. In previous documentation, the STP2210QFP was code named RISC.

BLOCK, LOGICAL, AND TYPICAL APPLICATION DIAGRAMS

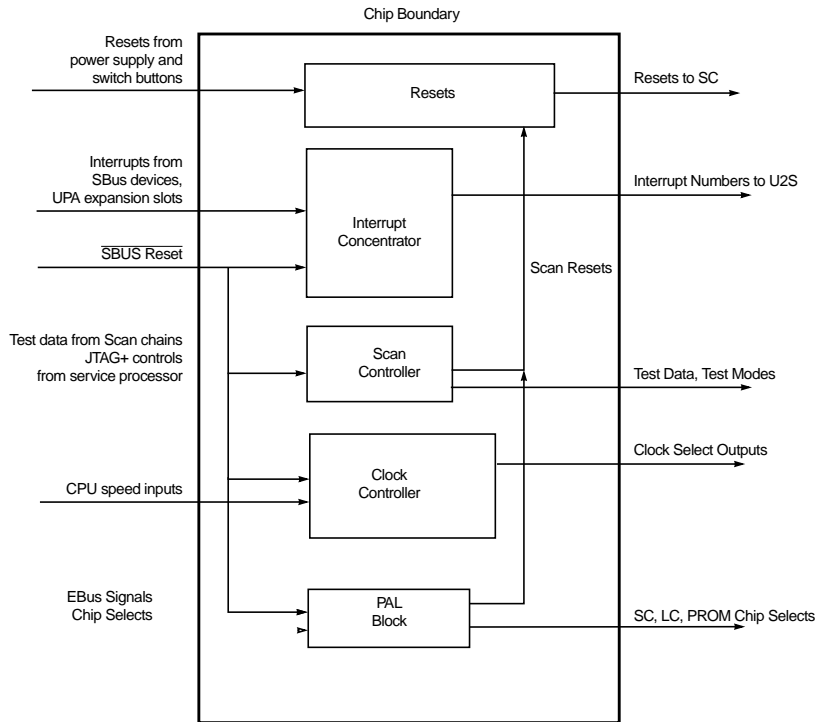


Figure 1. STP2210QFP Block Diagram

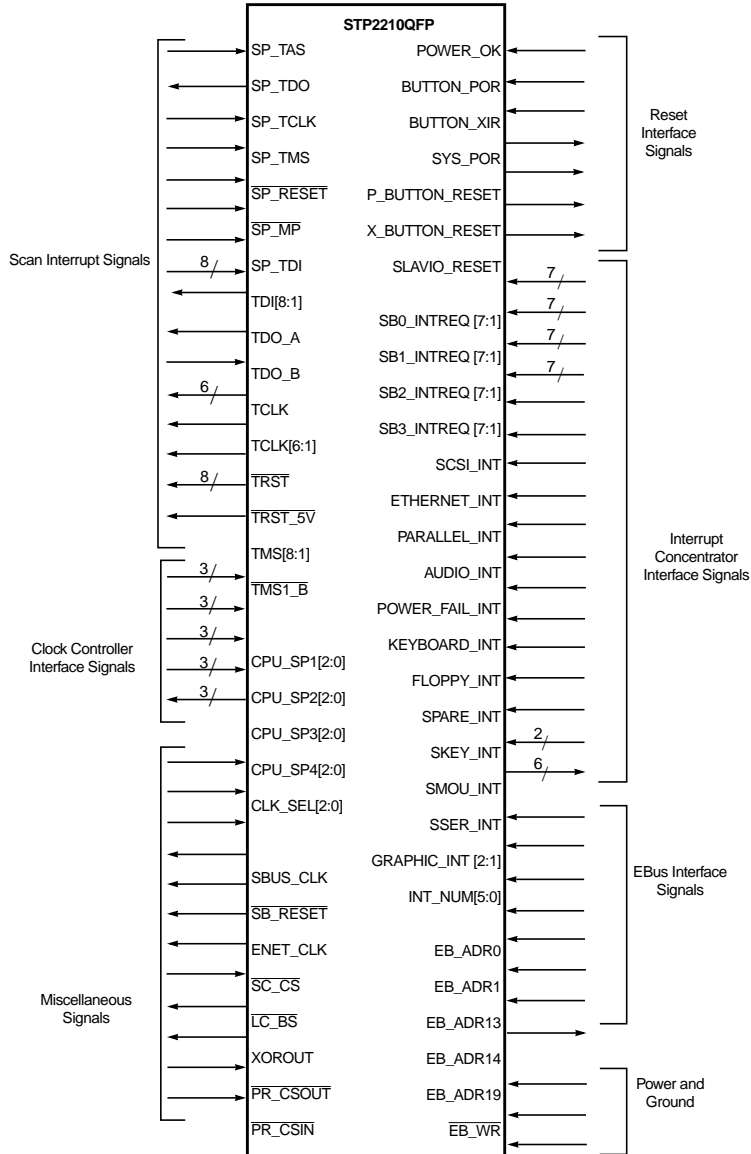


Figure 2. STP2210QFP Logical Connections

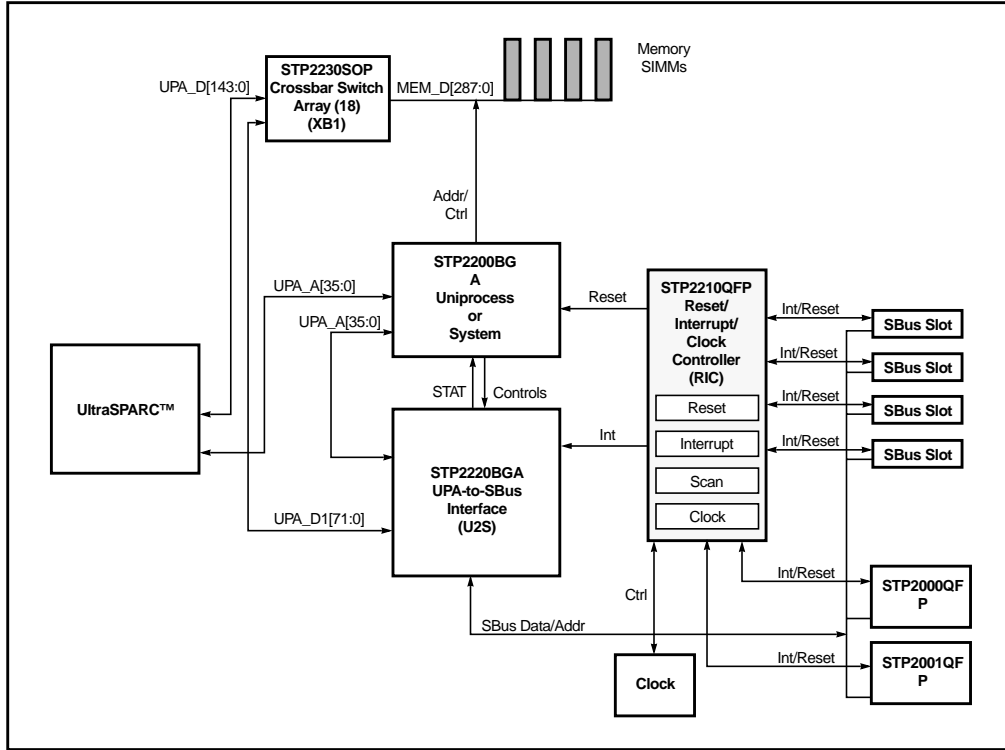


Figure 3. STP2210QFP Typical Application Diagram

SIGNAL DESCRIPTIONS

Reset Interface Signals

Signal	Pin Count	I/O	Description
POWER_OK	1	Input	Power-on reset from power supply
BUTTON_POR	1	Input	Signal asserted by push button reset
BUTTON_XIR	1	Input	Signal asserted by push button switch
SYS_POR	1	Output	Signal to STP2200BGA (USC) during power-on reset
P_BUTTON_RESET	1	Output	Signal to USC asserted during push button power reset
X_BUTTON_RESET	1	Output	Signal to USC asserted during push button XIR
SLAVIO_RESET	1	Output	Signal to reset STP2001 (SLAVIO)
TOTAL	7		

Interrupt Concentrator Interface Signals

Signal	Pin Count	I/O	Description
SB0_INTREQ[7:1]	7	Input	Interrupts from SBus slot 0
SB1_INTREQ[7:1]	7	Input	Interrupts from SBus slot 1
SB2_INTREQ[7:1]	7	Input	Interrupts from SBus slot 2
SB3_INTREQ[7:1]	7	Input	Interrupts from SBus slot 3
SCSI_INT	1	Input	Interrupts from SCSI controller
ETHERNET_INT	1	Input	Interrupts from Ethernet controller
PARALLEL_INT	1	Input	Interrupts from parallel port
AUDIO_INT	1	Input	Interrupts from audio port
POWER_FAIL_INT	1	Input	Interrupts from power_fail
KEYBOARD_INT	1	Input	Interrupts from keyboard
FLOPPY_INT	1	Input	Interrupts from floppy
SPARE_INT	1	Input	Spare interrupt
SKEY_INT	1	Input	Interrupts from keyboard for future use
SMOU_INT	1	Input	Interrupts from mouse for future use
SSER_INT	1	Input	Interrupts from serial port for future use
GRAPHIC_INT[2:1]	2	Input	Interrupts from optional graphics boards
INT_NUM[5:0]	6	Output	Interrupt number to U2S
TOTAL	47		

Scan Interrupt Signals

Signal	Pin Count	I/O	Description
SP_TAS	1	Input	Test address strobe from service processor
SP_TDO	1	Output	Test data out for Scan from service processor
SP_TCLK	1	Input	Test clock for Scan from service processor
SP_TMS	1	Input	Test mode select for Scan from service processor
SP_RESET	1	Input	Test reset for Scan from service processor
SP_MP	1	Input	Signal indicates Scan controller is connected
SP_TDI	1	Input	Scan data in
TDI [8:1]	8	Input	Test data from ASICs
TDO_A	1	Output	Test data out to ASICs
TDO_B	1	Output	Duplicate of TDO_A
TCLK	1	Input	10-MHz clock
TCLK_[6:1]	6	Output	10-MHz clock out to all ASICs on board
TRST	1	Output	Reset for the TAP controller
TRST_5V	1	Output	5-V reset for the TAP controller
TMS[8:1]	8	Output	Test mode select for ASICs
TMS1_B	1	Output	Duplicate of TMS[1]
TOTAL	35		

Clock Controller Interface Signals

Signal	Pin Count	I/O	Description
CPU_SP1[2:0]	3	Input	Speed inputs from CPU1
CPU_SP2[2:0]	3	Input	Speed inputs from CPU2
CPU_SP3[2:0]	3	Input	Speed inputs from CPU3
CPU_SP4[2:0]	3	Input	Speed inputs from CPU4
CLK_SEL[2:0]	3	Output	Selection code to the clock chip
TOTAL	15		

EBus Interface Signals

Signal	Pin Count	I/O	Description
EB_ADR0	1	Input	EBus address
EB_ADR1	1	Input	EBus address
EB_ADR13	1	Input	EBus address
EB_ADR14	1	Input	EBus address
EB_ADR19	1	Input	EBus address
EB_W \bar{R}	1	Input	EBus write signal
EB_C \bar{S}	1	Input	EBus chip select signal
EB_RDY	1	Output	EBus ready signal
TOTAL	8		

Miscellaneous Signals

Signal	Pin Count	I/O	Description
SBUS_CLK	1	Input	25-MHz SBus clock
SB_RESE \bar{T}	1	Input	SBus reset from U2S
ENET_CLK	1	Input	10-MHz clock for reset counter
SC_C \bar{S}	1	Output	USC chip select
LC_B \bar{S}	1	Output	Lab console chip select
XOROUT	1	Output	XOR gate output
PR_CSOUT	1	Output	PROM chip select output
PR_CSIN	1	Input	PROM chip select in
S_LOAD	1	Output	Signal-to-clock generator to load
S_CLOCK	1	Output	Signal-to-clock generator
XOR_IN1	1	Input	Spare signal
XOR_IN2	1	Input	Spare signal
TOTAL	12		

Power and Ground

Signal	Pin Count	Description
V _{CC}	11	5.0-V DC supply voltage
V _{SS}	18	Ground
V _{DD}	7	3.3-V DC supply voltage
TOTAL	36	

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V _{CC}	5 V power supply voltage	- 0.5	6.0	V
V _{DD}	3.3 V power supply voltage	- 0.5	4.6	V
V _{IN}	Input voltage range	- 0.5	V _{CC} + 0.5	V
P _D	Maximum power dissipation		0.5	W
T _{ST}	Storage temperature	- 65	150	°C
T _{CM}	Maximum case temperature		85	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{DD}	Supply voltage	3.15	3.3	3.45	V
T _{CO}	Operating case temperature	0		70	°C
F _{OSC}	Frequency of operation		25		MHz
I _{IN}	Input current	-10		+10	μA

Capacitance

Symbol	Parameter	Min	Max	Units
C _{IN}	Input capacitance	5	10	pF
C _{OUT}	Output capacitance	20	30	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IL}	Voltage input low				0.8	V
V _{IH}	Voltage input high		2.0			V
I _{IN}	Input current		- 10		+ 10	μA
I _{OUT}	Output current		- 2.0		+ 2.0	mA ⁽¹⁾
V _{OH}	Voltage output high		2.4			V
V _{OL}	Voltage output low				0.4	V

1. I_{OUT} min is I_{OH} MAX at V_{OH}
I_{OUT} max is I_{OL} max at V_{OL}

AC Characteristics (Input Signals)

Signal Name	Reference	Rise Time	Fall Time	Units
EB_ADR[0,1,13,14,19]	SBUS_CLK	3	3	ns
EB_ADR[0,1,13,14,19]	TCLK	3	3	ns
$\overline{\text{EB_WR}}$	SBUS_CLK	3	3	ns
$\overline{\text{EB_WR}}$	TCLK	3	3	ns
$\overline{\text{EB_CS}}$	SBUS_CLK	3	3	ns
$\overline{\text{EB_CS}}$	TCLK	3	3	ns
$\overline{\text{PR_CSIN}}$	TCLK	3	3	ns
SP_TAS	TCLK	5	5	ns
SP_MP	TCLK	5	5	ns
SP_TDI	TCLK	5	5	ns
SP_TMS	TCLK	5	5	ns
SP_RESET	TCLK	5	5	ns
TDI [8:1]	TCLK	5	5	ns

AC Characteristics (Input Signals)

Signal Name	Reference	Setup Time	Hold Time	Units
EB_ADR [0,1,13,14,19]	SBUS_CLK	25	5	ns
EB_ADR [0,1,13,14,19]	TCLK	25	5	ns
EB_WR	SBUS_CLK	25	5	ns
EB_WR	TCLK	25	5	ns
EB_CS	SBUS_CLK	25	5	ns
EB_CS	TCLK	25	5	ns
PR_CSIN	TCLK	25	5	ns
SP_TAS	TCLK	60	50	ns
SP_MP	TCLK	N/A	N/A	ns
SP_TDI	TCLK	60	50	ns
SP_TMS	TCLK	60	50	ns
SP_RESET	TCLK	60	50	ns
TDI [8:1]	TCLK	70	50	ns

AC Characteristics (Output Signals)

Signal Name	Reference	Propagation Delay (Maximum)	Units
INT_NUM [5:0]	SBUS_CLK	23	ns
INT_NUM [5:0]	TCLK	40	ns
SLAVIO_RESET	SBUS_CLK	23	ns
SLAVIO_RESET	TCLK	40	ns
PR_CSOUT	SBUS_CLK	23	ns
PR_CSOUT	TCLK	40	ns
EB_RDY	SBUS_CLK	23	ns
EB_RDY	TCLK	40	ns
S_LOAD	SBUS_CLK	23	ns
S_LOAD	TCLK	40	ns
S_CLOCK	SBUS_CLK	23	ns
S_CLOCK	TCLK	40	ns
SC_CS	SBUS_CLK	23	ns
SC_CS	TCLK	40	ns
LC_BS	SBUS_CLK	23	ns
LC_BS	TCLK	40	ns
XOROUT	SBUS_CLK	23	ns
XOROUT	TCLK	40	ns

AC Characteristics (Output Signals)

Signal Name	Reference	Propagation Delay (Maximum)	Units
SYS_POR	SBUS_CLK	25	ns
$\overline{\text{SYS_POR}}$	TCLK	40	ns
P_BUTTON_RESET	SBUS_CLK	25	ns
$\overline{\text{P_BUTTON_RESET}}$	TCLK	40	ns
X_BUTTON_RESET	SBUS_CLK	25	ns
$\overline{\text{X_BUTTON_RESET}}$	TCLK	40	ns
CLK_SEL [2:0]	CPU_SP [4:1]	25	ns
SP_TDO	TCLK	25	ns
TDO_A	TCLK	25	ns
TDO_A	SP_TDI	20	ns
TDO_B	TCLK	25	ns
TDO_B	SP_TDI	20	ns
TMS[8:1]	TCLK	25	ns
$\overline{\text{TRST}}$	TCLK	45	ns
$\overline{\text{TRST}}$	ENET_CLK	45	ns
$\overline{\text{TRST_5V}}$	TCLK	45	ns
$\overline{\text{TRST_5V}}$	ENET_CLK	45	ns
TCLK_[6:1] ⁽¹⁾	SP_TCLK	23	ns

1. The skew between TCLK_1 to TCLK_6 must be 1 ns or less.

Clock Signal Input Specifications

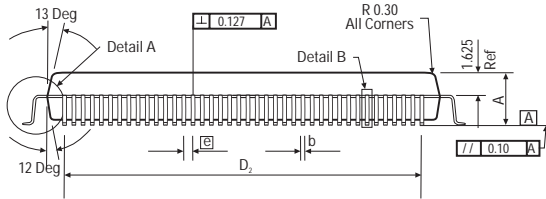
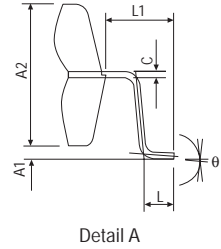
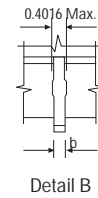
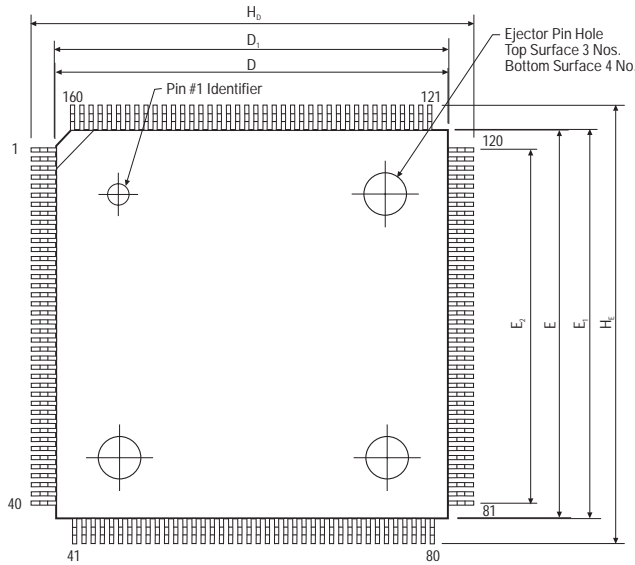
Clock Name	DC Levels				Rise/Fall Time		Duty Cycle		Sync or Async
	Period (Min) (ns)	T _{OL} (Max) (ns)	V _{IL} (Max) (V)	V _{IH} (Min) (V)	Rise Time (Max) (ns)	Fall Time (Max) (ns)	HIGH (Min) (ns)	LOW (Min) (ns)	
SBUS_CLK	30	1	0.8	2.0	1	1	17	13	Async
ENET_CLK	100	5	0.8	2.0	1	1	50	50	Async
$\overline{\text{TCLK}}$	100	2	0.8	2.0	1	1	50	50	Async

PACKAGE INFORMATION

160-Pin QFP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	vss	33	SB3_INTREQ5	65	SLAVIO_RESET	97	TDI6	129	CLK_SEL1
2	SB0_INTREQ1	34	SB3_INTREQ6	66	vss	98	TDI7	130	CLK_SEL2
3	SB0_INTREQ2	35	SB3_INTREQ7	67	CPU_SP1_0	99	TDI8	131	V _{DD}
4	SB0_INTREQ3	36	V _{DD}	68	CPU_SP1_1	100	TCLK_1	132	S_CLOCK
5	SB0_INTREQ4	37	CPU_SP4_0	69	CPU_SP1_2	101	vss	133	BUTTON_POR
6	V _{CC}	38	CPU_SP4_1	70	CPU_SP2_0	102	TDO_A	134	BUTTON_XIR
7	SB0_INTREQ5	39	CPU_SP4_2	71	V _{DD}	103	TDO_B	135	EB_ADR0
8	SB0_INTREQ6	40	vss	72	CPU_SP2_1	104	TCLK_2	136	vss
9	SB0_INTREQ7	41	V _{CC}	73	CPU_SP2_2	105	TCLK_3	137	EB_ADR1
10	SB1_INTREQ1	42	SCSI_INT	74	CPU_SP3_1	106	V _{DD}	138	EB_ADR13
11	vss	43	ETHERNET_INT	75	CPU_SP3_2	107	TMS1	139	EB_ADR14
12	SB1_INTREQ2	44	PARALLEL_INT	76	vss	108	TMS2	140	EB_ADR19
13	SB1_INTREQ3	45	GRAPHIC_INT[1]	77	CPU_SP3_0	109	TMS3	141	V _{CC}
14	SB1_INTREQ4	46	vss	78	SB_RESET	110	TMS4	142	EB_WR
15	SB1_INTREQ5	47	AUDIO_INT	79	TRST_5V	111	vss	143	EB_CS
16	V _{CC}	48	POWER_FAIL_INT	80	V _{CC}	112	TMS5	144	EB_RDY
17	SB1_INTREQ6	49	GRAPHIC_INT[2]	81	vss	113	TMS6	145	PR_CSIN
18	SB1_INTREQ7	50	KEYBOARD_INT	82	SP_TDO	114	TMS7	146	vss
19	SB2_INTREQ1	51	V _{CC}	83	SP_TAS	115	TMS8	147	PR_CSOUT
20	SB2_INTREQ2	52	FLOPPY_INT	84	SP_MP	116	V _{DD}	148	TMS1_B
21	vss	53	SPARE_INT	85	SP_TDI	117	TCLK_4	149	POWER_OK
22	SB2_INTREQ3	54	SKEY_INT	86	V _{CC}	118	TCLK_5	150	V _{CC}
23	SB2_INTREQ4	55	SMOU_INT	87	SP_TCLK	119	TCLK_6	151	XOR_IN1
24	SB2_INTREQ5	56	vss	88	SP_TMS	120	vss	152	XOR_IN2
25	SB2_INTREQ6	57	SSER_INT	89	SP_RESET	121	V _{DD}	153	XOROUT
26	V _{CC}	58	INT_NUM0	90	TDI1	122	S_LOAD	154	SC_CS
27	SB2_INTREQ7	59	INT_NUM1	91	vss	123	TRST	155	LC_BS
28	SB3_INTREQ1	60	INT_NUM2	92	TDI2	124	SYS_POR	156	vss
29	SB3_INTREQ2	61	V _{CC}	93	TDI3	125	P_BUTTON_RESET	157	ENET_CLK
30	SB3_INTREQ3	62	INT_NUM3	94	TDI4	126	vss	158	TCLK
31	vss	63	INT_NUM4	95	TDI5	127	X_BUTTON_RESET	159	SBUS_CLK
32	SB3_INTREQ4	64	INT_NUM5	96	V _{DD}	128	CLK_SEL0	160	V _{CC}

160-Pin PQFP Package Dimensions



Dimension	mm	Dimension	mm
A	Min	3.42	D2 Ref 25.35
	Nom	3.73	E Min 27.70
	Max	4.07	Nom 27.80
A1	Min	0.25	Max 27.90
	Nom	0.33	E1 Min 27.90
	Max	0.40	Nom 28.00
A2	Min	3.17	Max 28.10
	Nom	3.40	E2 Ref 25.35
	Max	3.67	e BSC 0.65
B	Min	0.25	HD Min 30.95
	Nom	0.30	Nom 31.20
	Max	0.38	Max 31.45
C	Min	0.13	HE Min 30.95
	Nom	0.15	Nom 31.20
	Max	0.23	Max 31.45
D	Min	27.70	L Min 0.65
	Nom	27.80	Nom 0.80
	Max	27.90	Max 0.95
D1	Min	27.90	L1 Nom 1.60
	Nom	28.00	theta Min 0
	Max	28.10	Max 7

- Note:
- Total number of pins is 160.
 - Drawing is not to scale.
 - Molding flash is permitted around periphery of body. Flash shall not extend more than 0.254 mm beyond body.
 - This drawing is for cavity mold only.

ORDERING INFORMATION

Part Number	Description
STP2210QFP	Reset/Interrupt/Clock Controller (RIC)

Document Part Number: 805-0166-02