

UltraSPARC™-III

User's Manual—Addendum

*For Use with UltraSPARC-III User's Manual
805-0087-01*



THE NETWORK IS THE COMPUTER™

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UltraSPARC-IIi Enhancements

This addendum is meant to be used in conjunction with The *UltraSPARC-IIi User's Manual*: 805-0087-01 (this addendum applies to). It explains the additional features and differences between the original SME1040 UltraSPARC-IIi (Sabre) CPU, and the SME1430LGA (Sapphire Red) CPU. This accounting of the changes is to appear in the forthcoming UltraSPARC-IIi User's Manual 805-0087-02 (updated version).

Following brief descriptions of the enhancements of the SME1430LGA product—both at the chip and CPU module level—this addendum includes the revised Chapter 18, *MCU Control and Status Registers* that is to appear integrated into the *User's Manual* update. Note that page numbers and cross-references that appear in this section are aligned with pages in the forthcoming -02 update. However, most of the sections can be found on nearly-corresponding pages in the current manual.

SME1430LGA CPU Enhancements Over the SME1040CGA CPU

Both SME1430LGA and SME1040CGA UltraSPARC-IIi CPU processors are housed in the same LGA package but the SME1430LGA chip contains functional improvements.

Electrical and Thermal Differences

- Core supply voltage V_{dd_core} is reduced from 2.6 V to 1.9 V.
- Power consumption is reduced at a given frequency with an associated reduction in heat dissipation.
- The CPU runs at a reduced junction temperature T_j .

Functional Differences

Synchronizer Stages

Pin P03 has been redefined to SYNC_3TO1_MODE.

This function was added to allow for a third synchronizer stage should it prove necessary to ensure stability. In fact, this feature proved unnecessary and it is recommended that this pin be strapped to ground causing the processor to operate as the SME1040CGA in this regard.

The UltraSPARC-II*i* CPU has a time domain boundary between the CPU core and the PCI primary bus interface. This pin controls the number of CPU clocks that the CPU waits for the synchronizers to settle. If set to a 1, the CPU waits for 3 CPU clock cycles. If set to a 0, the CPU waits two CPU clocks. This pin has a weak internal pull down resistor that is enabled during RAMTEST and RESET modes.

CPU to UPA Clock Frequency Ratio

The CPU to UPA clock ratio is fixed by design. In the SME1040CGA the ratio is always 3:1. In SME1430LGA, the ratio is 4:1.

Memory Controller Bits

A number of timing template bits and their definitions in Mem_Control0 and Mem_Control1 registers have changed to support higher internal clock rates with the same DIMM timing. For details, refer to the addendum to the UltraSPARC-II*i* User's Manual.

Enhancements in the SME543xPCI CPU Module Compared with the SME5421MCZ Version

There are minor changes to the II*i* CPU module for SME1430LGA (sapphire red).

Both the SME1430LGA and the SME1040CGA UltraSPARC-II*i* processors are housed in the same LGA package. The SME1430LGA CPU used in this module contains functional improvements. This module also employs a heatsink of revised design but the overall dimensions remain as before.

Electrical and Thermal Differences

Voltage Requirements

CPU core supply voltage V_{DD_CORE} is reduced from 2.6 V to 1.9 V. This change is achieved by implementing the appropriate resistor stuffing configuration in the module to set the VID[4:0] bits on the system board. See the module datasheet listed in *References*.

Power Consumption

Power consumption is reduced at a given frequency with an associated reduction in heat dissipation.

Temperature and Cooling

The CPU runs at a reduced junction temperature T_j . The module heatsink is changed to a straight-fin design. This requires airflow in line with the fin. See the module datasheets for thermal information.

Functional Differences

UPA Bus Frequency

The UPA bus is clocked at 1/4 the CPU core frequency

Memory Controller

A number of timing template bits in Mem_Control0 and Mem_Control1 registers have changed to support higher internal clock rates with the same DIMM timing. For details, refer to the Chapter 18 update in the succeeding pages of this addendum.

References

Datasheets

UltraSPARC-III CPU; Highly Integrated 64-bit RISC; L2-Cache; DRAM, PCI Interface, SME1430: 805-7291

UltraSPARC-IIi CPU Module; 360/440/480 MHz CPU; 0.25 to 2 MB L2 Cache, UPA64S, 66 MHz PCI; SME5431PCI-360; SME5431PCI-440; SME5431PCI-480; 806-0480

UltraSPARC-III Highly Integrated 64-bit RISC Processor, PCI Interface, SME1040: 805-0086

User's Manuals

UltraSPARC-III User's Manual, 805-0087-01 (this addendum applies)

UltraSPARC-III User's Manual, 805-0087-02 (no addendum required)

MCU Control and Status Registers

The MCU control and status registers program the operation of the shared memory and UPA64S interfaces which are integrated into the UltraSPARC-II*i* CPU.

Register Access

Register accesses should always be of eight bytes at a time. The Physical addresses for the MCU control and status registers are shown in *Table 18-1*.

Table 18-1 MCU CSRs

PA	Register Name	Associated I/O Port
1FE.0000.F000	FFB_Config	FFB
1FE.0000.F010	Mem_Control0	Memory Control Unit
1FE.0000.F018	Mem_Control1	Memory Control Unit

Reads of any size up to eight byte to any register are supported regardless of whether reads of that size makes sense.

Writes of any size up to eight bytes are also supported regardless of whether writes of that size makes sense. Writes of any size *may* corrupt unwritten bits in the register. (that is., writes may result in all eight bytes being written regardless of the indicated write size.)

Software must ensure that only the proper-sized—that is, equal to the register size—accesses are used. No hardware checking is performed. Block (64-byte) access erroneously causes a UPA64S or PCI transaction with an undefined address.

Misaligned access due to not setting the “E” bit correctly in the TTE also yields unpredictable results.

Note – Register bits that are designated as read only (RO) are not affected by writes. No errors are reported. Fields with reserved definitions should not be used. Some combinations of bits are not valid. Disable refresh before changing memory control registers.

Compatibility Note – Prior UltraSPARC-based systems used other hardware and programming models to control the UPA and memory interfaces.

Reset

Memory Control registers are reset to their initial values only during PowerOnReset (POR). POR is often generated by logic connected to the POWER_OK signal from the power supply. Refreshing operates continuously during and after other reset conditions.

The SYS_RESET signal is asserted by the system POR condition. The P_RESET signal is asserted for many reasons and does not affect many of the memory control register bit values.

Table headings with POR mean the register is affected by SYS_RESET only. Table headings with Reset mean the register is affected by SYS_RESET or P_RESET.

18.1 FFB_Config Register

Table 18-2 FFB_Config Register—0x1FE.0000.F000

Field	Bits	Description	Reset	Type
Reserved	63:28		0	RO
SPRQS	27:24	Slave P_request queue size. Initialize to max size in 2 Cycle Packets of the corresponding slave request queue.	1	R/W
Reserved	23:15		0	RO
Oneread	14	Always set to 'one'; UPA slave interface does not support multiple outstanding reads.	1	RO
Reserved	13:0		0	RO

The Data Queue Size is not tracked separately, and the UPA64S device must be able to receive 64 bytes per allowed outstanding request.

18.2 Mem_Control0 Register

Table 18-3 Mem_Control0 Register—0x1FE.0000.F010

Field	Bits	Description	POR	Type
Reserved	63:32		0	RO
RefEnable	31	Refresh enable	0	R/W
Reserved	30:29		0	RO
ECCEnable	28	Enable all ECC functions	0	R/W
Trace_Delay	27	SME1430: short trace enable	0	R/W
Reserved	27	SME1040	0	R/W
FFBwrToDRAMrdDly	26:25	SME1430: memdata bus turnaround	0	R/W
Reserved	24:13	SME1430		RO
Reserved	26:13	SME1040	0	RO
11-bit Column Address	12	Enables 11-bit column address mode.	0	R/W
DIMMPairPresent<3:0>	11:8	Determines which DIMM pairs to refresh.	0xF	R/W
RefInterval<7:0>	7:0	Interval between refreshes. Each encoding is 32 processor clocks	0x30	R/W

ECCEnable

This instruction enables the MCU to perform single-bit detect and correct, and notification of single or multi-bit errors to the ECU and PBM, for possible logging and trap/interrupt generation. In general this should always be set to 1, unless DIMMs that do not support check bits are used.

There are further enables for ECC related trap and interrupt generation in the ECU and PBM. See Section 16.6.1, *E-cache Error Enable Register* on page 240 and DMA UE/CE interrupt mapping registers in *Partial Interrupt Mapping Registers* on page 301 and ERRINT_EN in *PCI Control/Status Register* on page 281.

Trace Delay (SME1430 only)

Trace_Delay is defined in mem_control1<27>. Set to 1 for SME1040 type timing. Set to 0 for shorter trace delays. This bit defaults to 0 at power-up. The impact on programming is shown in the Mem_Control1 Register RCD field—see page 272 and the FFBwrToDRAMrdDly section below.

FFBwrToDRAMrdDly (SME1430 only)

FFBwrToDRAMrdDly is defined in mem_control1<26:25>. An FFB write operation followed by a DRAM read operation is optimized by using this 2-bit field. This bit field value is adjusted according to CPU clock rate and DRAM speed.

FFBwrToDRAMrdDly value adjusts the delay in the initiation of a DRAM read after an FFB write operation so that there is no collision on the memory bus between data returning from DRAM and data written to the FFB. The value “11” gives the smallest delay whereas the value “00” gives the largest delay. *Table 18-4* shows the use of FFBwrToDRAMrdDly for various configurations of processor frequency and setting of CASRW.

Table 18-4 Use of FFBwrToDRAMrdDly

Processor Frequency	CASRW	Trace_Delay=0	Trace_Delay=1
360	4	01 ¹	na ²
	5	01	10
400	4	11 ¹	na
	5	11	11
440	5	10 ¹	na
	6	10	10
480	5	10 ¹	na
	6	11	11

1. requires 50 ns DRAMs
2. not applicable or valid

RefEnable

Main memory is composed of dynamic RAMs, which require periodic “refreshing” to maintain the contents of the memory cells. RefEnable == 1 is used to enable refresh of main memory. RefEnable == 0 disables refresh in memory.

POR is the only reset condition that clears RefEnable (and initializes the rest of the Mem_Control0/1). SOFT_POR, B_POR, B_XIR, and SOFT_XIR leave RefEnable unchanged and refresh continues normally.

Any refresh operation in progress is aborted at the time of clearing this bit. The truncated memory signals in this case could lead to loss of data.

11-bit Column Address

The default memory addressing only supports 10-bit column address DRAMs. An additional mode was added to support a 11-bit column address. Since the total available address bits in the memory controller is constant (1 Gbyte max. addressable), the maximum number of DIMM pairs in this mode is cut in half. See Chapter 7, *UltraSPARC-III Memory System*.

DIMMPairPresent<3:0>

Indicates the presence/absence of DIMMS to enable performance degradation caused by refreshing unpopulated DIMMs to be eliminated. One bit position corresponds to each DIMM bank. “DIMM pair 0” corresponds to “DimmPairPresent[0],” and so on. A zero indicates not present, a 1 indicates present. These bits are set by software after probing. Note that in 11-bit Column Address mode, only DIMM Pair 0 and 2 can be marked present. Pairs 1 and 3 should always be marked not present when in 11-bit column addressing mode.

Note – Refresh must be disabled first by clearing the RefEnable bit before changing the memory controller register values. Refresh may be enabled again simultaneously with writing DIMMPairPresent and RefInterval. Failure to follow this rule may result in unpredictable behavior.

Table 18-5 Various Memory Configurations

DIMM size	Base device	No. of devices	System memory min/max config
8 MB	1M x 4	18	16 MB/64 MB
16 MB	2M x 8	9	32 MB/128 MB
32 MB	4M x 4	18	64 MB/256 MB
64 MB	4M x 4(banked)	36	128 MB/512 MB
64 MB	8M x 8	9	128 MB/512 MB

Table 18-5 Various Memory Configurations (*Continued*)

DIMM size	Base device	No. of devices	System memory min/max config
128 MB	8M x 8(banked)	18	256 MB/1 GB
128 MB	16M x 4	18	256 MB/1 GB
256 MB	16M x 4(banked)	36	512 MB/1 GB

RefInterval

RefInterval specifies the interval time between refreshes, in quanta of 32 CPU clocks. SW should program RefInterval according to *Table 18-6*. Values given are in hexadecimal and derived from this formula:

$$refValue = \frac{refreshPeriod}{numberOfRows \times ClockPeriod \times 32 \times numberOfPairs}$$

that is: (32 * frequency * 1000) / (2048 * 32 * DIMM pairs).

This data is based on using 16 MB(2048 rows/32ms) EDO drams only; this configuration matches the composite DIMM specification. See *Table 18-6*.

Table 18-6 Refresh Period (in 32x CPU clock periods) as a Function of Frequency

Total DIMM pairs enabled	CPU Frequency in MHz											
	125–166	167–200	201–224	225–250	251–270	271–300	301–330	331–360	361–400	401–440	441–450	451–480
1	0x51	0x61	0x6C	0x7A	0x83	0x92	0xA1	0xAF	0xC3	0xD6	0xDB	0xEA
2	0x28	0x30	0x37	0x3D	0x41	0x49	0x50	0x57	0x61	0x6B	0x6D	0x75
3	0x1B	0x20	0x25	0x28	0x2B	0x30	0x35	0x3A	0x41	0x47	0x49	0x4E
4	0x14	0x18	0x1D	0x1E	0x20	0x24	0x28	0x2B	0x30	0x35	0x36	0x3A

18.3 Mem_Control1 Register

Memory Control Register 1 contains fields that control the read, write, and refresh timing for the DRAM DIMMs. They allow software to optimize the memory access timing for a particular system frequency.

The contents of Memory Control Register 1 can be changed as required by an electrical tuning of memory timing often based on SPICE analysis. The Mem_Control1 register bits are listed in *Table 18-7*.

Table 18-7 Mem_Control1 Register—0x1FE.0000.F018

Field	Bits	POR State	Description	Type
Reserved	63:32	0	reserved. Read as zero, write 0	RO
AMDC<3>	31	0	SME1430 Advance Memdata Clock	R/W
ARDC<3>	30	0	SME1430 Advance Read Data Clock	R/W
Reserved	31:30	0	SME1040 reserved; read as zero, write 0	RO
AMDC<2:0>	29:27	0	Advance Memdata Clock	R/W
ARDC<2:0>	26:24	0	Advance Read Data Clock	R/W
CSR ¹	23:21	2	CAS to RAS delay for CBR refresh cycles.	R/W
CASRW ^{1, 2}	20:18	2	CAS length for read/write	R/W
RCD ¹	17:15	4	RAS to CAS Delay	R/W
CP	14:12	2	CAS Precharge	R/W
RP ¹	11:9	4	RAS Precharge	R/W
RAS ¹	8:6	5	Length of RAS for Refresh	R/W
CASRW ^{1, 2}	5:3	2	Must be same as 20:18	R/W
RSC ²	2:0	0	RAS after CAS hold time	R/W

1. Bit definitions differ between SME1430 and SME1040. See bit-definition sections that follow

2. Originally had separate fields for CAS during reads and CAS during writes. However, memory timing is optimal if writes and reads use the same CAS width. Additionally, an errata caused the read CAS width to be used in one part of the write control logic. Both fields are now given the same name, and must be programmed to the same value. Results are undefined if they are different.

Even though many bits are set by reset, it is good practice to have the boot PROM program all memory control register bits when initializing the system.

AMDC- Advance Memdata Clock

This instruction moves the relative timing between a transceiver clock transition and the point at which the processor latches read data driven by that transceiver (using the MEMDATA bus)

This timing adjustment allows for earlier data clocking for slower clock cycles. (advance) or for later data clocking for fast clock cycles.

Delaying this clocking by a cycle (relative to the recommended values) may be useful if timing is critical but it reduces hold time margin.

Table 18-8 AMDC Timing Arguments—Mem_Control1<31>,<29:27>

Argument	SME1040	SME1430	Timing
0000	0	0	default MemData clocking
0001	1	1	CPU clocks of sampling delay
0010	2	2	CPU clocks of sampling delay
0011	3	3	CPU clocks of sampling delay
0100	4	4	CPU clocks of sampling advancement
0101	3	3	CPU clocks of sampling advancement
0110	2	2	CPU clocks of sampling advancement
0111	1	1	CPU clocks of sampling advancement
1000–1010	reserved	reserved	
1011	reserved	5	CPU clocks of sampling advancement
1100–1111	reserved	reserved	

ARDC- Advance Read Data Clock

Maintaining a minimum EDO DRAM CAS cycle is difficult if the DIMM loading is widely variable. Light loading on the CAS and DATA lines can make the data disappear before it is clocked and produce a hold-time problem.

The system board reference design specifies buffering to make the RAS/CAS/WE delays independent of the number of DIMMs in circuit. However, the ADDR and DATA delays do vary with DIMM population.

If necessary, this field can be used to advance the clock that latches read data in the transceivers. This may be necessary when only one or two DIMM pairs are populated. It can also be used to delay the clock for heavily loaded DIMM populations.

Current simulations indicate that the ARDC value need not be varied for the supported range and combinations of DIMM configurations.

Table 18-9 ARDC Timing Arguments—Mem_Control1<30>,<26:24>

Argument	SME1040	SME1430	Timing
0000	0	0	default DRAM Read data clocking based on CAS assertion time
0001	1	1	CPU clocks of sampling delay
0010	2	2	CPU clocks of sampling delay

Table 18-9 ARDC Timing Arguments—Mem_Control1<30>, <26:24> (Continued)

Argument	SME1040	SME1430	Timing
0011	3	3	CPU clocks of sampling delay
0100	4	4	CPU clocks of sampling advancement
0101	3	3	CPU clocks of sampling advancement
0110	2	2	CPU clocks of sampling advancement
0111	1	1	CPU clocks of sampling advancement
1000	reserved	8	CPU clocks of sampling advancement
1001	reserved	7	CPU clocks of sampling advancement
1010	reserved	6	CPU clocks of sampling advancement
1011	reserved	5	CPU clocks of sampling advancement
1100–1111	reserved	reserved	

CSR - CAS before RAS delay timing

This Instruction controls the CAS assertion to RAS assertion delay for CAS before RAS (CBR) refresh cycles

Table 18-10 CSR Delay Timing—Mem_Control1<23:21>

Argument	SME1040	SME1430	Timing
000	3	3	CPU clocks between CAS and RAS assertions
001	4	4	CPU clocks between CAS and RAS assertions
010	5	5	CPU clocks between CAS and RAS assertions
011	6	6	CPU clocks between CAS and RAS assertions
100	7	7	CPU clocks between CAS and RAS assertions
101	8	8	CPU clocks between CAS and RAS assertions
110	reserved	2	CPU clocks between CAS and RAS assertions
111	reserved	reserved	

CASRW- CAS assertion for read/write cycles

CASRW controls the minimum CAS assertion time for reads and writes.

There were originally separate fields for CAS during reads and CAS during writes. However, memory timing is optimal if writes and reads use the same CAS width. Additionally, an erratum caused the read CAS width to be used in one part of the write control logic. Both fields are now given the same name, and must be programmed to the same value. Results are undefined if they are different.

Table 18-11 CASRW Assertion Time—Mem_Control1<20:18> (same settings at <5:3>)

Argument	SME1040	SME1430	Timing
000	3	reserved	clocks for which CAS is in low state
001	4	4	clocks for which CAS is in low state
010	5	5	clocks for which CAS is in low state
011	reserved	6	clocks for which CAS is in low state
100-111	reserved	reserved	

RCD - RAS to CAS Delay

RCD controls the RAS to CAS delay during the initial part of the read or write memory cycle.

In the SME1430, the RCD operation is determined by the RCD and Trace_Delay (Mem_Control1<27>) values.

Table 18-12 RCD Delay Timing—Mem_Control1<17:15>

Argument	SME1040	SME1430		Timing
		Trace_Delay=1	Trace_Delay=0	
000	6	13	13	
001	7	17	17	
010	8	20	19	
011	11	11	12	CPU clocks between RAS and CAS assertion
100	12	19	18	
101	14	14	14	
110	15	15	15	
111	reserved	reserved	reserved	

CP - CAS Precharge

CP controls the CAS precharge time in between page cycles. The argument in this field must equal the common argument in each CASRW field.
(Mem_Control1<20:18> and Mem_Control1<5:3>)

Table 18-13 CP - CAS Precharge Time—Mem_Control1<14:12>

Argument	SME1040	SME1430	Timing
000	3	reserved	CPU clocks of CAS Precharge
001	4	4	CPU clocks of CAS Precharge
010	5	5	CPU clocks of CAS Precharge
011	reserved	6	
100-111	reserved	reserved	

RP - RAS Precharge

RP controls the RAS precharge time between memory cycles.

Table 18-14 RP Timing—Mem_Control1<11:9>

Argument	SME1040	SME1430	Timing
000	8	12	
001	9	13	
010	10	21	
011	11	17	CPU clocks of RAS Precharge
100	12	19	
101	14	14	
110	15	15	
111	reserved	16	

RAS

RAS is used to control the length of time that RAS is asserted during refresh cycles.

Table 18-15 RAS Duration Time—Mem_Control1<8:6>

Argument	SME1040	SME1430	Timing
000	13	20	
001	15	15	
010	18	18	
011	22	22	
100	23	23	CPU clocks of RAS assertion.
101	24	24	
110	reserved	27	
111	reserved	31	

RSC-RAS after CAS delay timing

RSC controls time to deassert RAS after CAS at the end of a memory cycle.

Table 18-16 RSC - RAS Deassert Time—Mem_Control1<2:0>

Argument	SME1040	SME1430	Timing
000	4	4	CPU clocks RAS asserted after CAS
001	5	5	CPU clocks RAS asserted after CAS
010	6	6	CPU clocks RAS asserted after CAS
011	7	7	CPU clocks RAS asserted after CAS
100	8	8	CPU clocks RAS asserted after CAS
101	9	9	CPU clocks RAS asserted after CAS
110	reserved	10	CPU clocks RAS asserted after CAS
111	reserved	reserved	

18.4 Programming Mem_Control1

Table 18-17 gives program values to support one, two, three, or four DIMM pairs, with one or two banks of DRAM on each DIMM. These values are given as a function of the internal CPU operating frequency.

These tabulated values depend upon the conditions:

- The system board meeting the min/max delay specifications for RAS/CAS/MEMADDR/DATA/MEMDATA, and all transceiver control and clock signals;
- The design specifications for max skew between RAS/CAS/MEMADDR/DATA being met.
- The specified DIMMs being used. (buffered CAS/WE/ADDR)

Memory Control Register programming may also be used to utilize memory subsystems whose performance lies outside the suggested design specifications.

Because all skew and hold time relationships for the DRAMs are not programmable, it is recommended that all designs meet the etch length specifications and employ DIMMs that meet the composite specification.

It is possible that alternate values may give higher performance from 50 ns DRAM. The minimum CAS cycle with this programming is 26.5 ns (13.25 ns CAS assertion) at 300 Mhz.

Table 18-17 Mem_Control1 hexadecimal values as a function of CPU frequency

CPU Frequency in MHz	SME1040 ²		SME1430 ³	
	60 ns DRAM	50 ns DRAM	60 ns DRAM	50 ns DRAM
480			5E28.25D3	4E69.AF93
450 to 479			544E.B9DA	4E69.A792
401 to 449			544C.B9DD	410A.AD54
361 to 400			0C4B.2794	0005.92CB
334 to 360	0C4A.AB14	0645.9ACB	0C4A.AB14	0645.9ACB
271 to 333	0645.9ACB	0645.9ACB	–	–
225 to 270	0626.168A	0626.168A	–	–
167 to 224	3800.8241	3800.8241	–	–
125 to 166	3E00.8000	3E00.8000	–	–
0-1 ¹	3D00.0000	5D00.0000	–	–

1. This programming is included for emulation. The PLLs should be bypassed, and an external means of supplying DRAM refresh should be provided.
2. Excepting the 334 to 360 MHz range, SME1040 programming for 50 and 60 ns DRAMs is currently the same. Either DRAM rating can be used with the same performance.
3. Speeds above 440 MHz have not been tested.

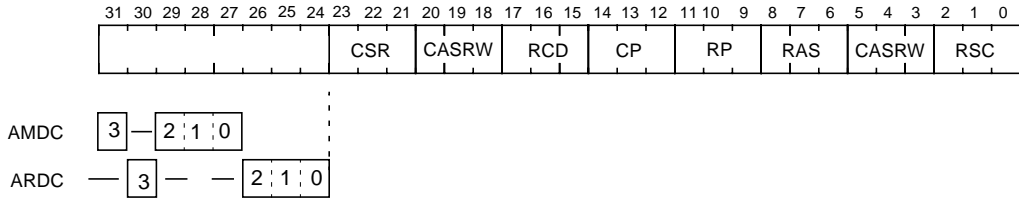


Figure 18-1 Mem_Control1 Register Bit Allocation

Initialization of the Mem_Control registers should be performed in accordance with the probing algorithm described in Section A.10, *Memory Probing and Initialization* on page 381.

Note – The Mem_Control register must be initialized before *any* memory operation, including refresh. Before modifying the register, software must complete and inhibit all memory references and disable refresh. Wait 100 clock periods after disabling refresh to guarantee completion of any refresh in progress.

18.5 UPA Configuration Register

The UPA_CONFIG register can be accessed at ASI 0x4A, VA==0. This is a 64-bit register; non-64-bit aligned accesses cause a *mem_address_not_aligned* trap.

Much of the UltraSPARC-I and UltraSPARC-II functionality in this register is removed.

UltraSPARC-IIi uses a register in the Memory Control Unit to restrict the number of outstanding UP64S slave requests, instead of this register.

The new ELIM field is copied from UltraSPARC-II.

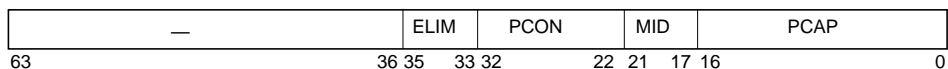


Figure 18-2 UPA_CONFIG Register Format

ELIM: This field can be used to zero upper bits of the E-cache tag address, if more address pins are used on the tag RAM than necessary. It can also be used to force the use of a smaller E-cache size than is supplied with the UltraSPARC-IIi system.

Resets to 000. Must be set to a size not bigger than the E-cache data SRAMs provide, otherwise incorrect E-cache operation will result.

000 has no effect on the E-cache tag address.

111 and 110 zero the 3 MSBs to create a 256-kilobyte E-cache, regardless of the SRAM size or connections to the E-tag.

101 allows a 512-kilobyte E-cache, if the SRAMs used are sized appropriately. Otherwise, the E-cache is the size allowed by the SRAMs.

100 allows a 1-Mbyte E-cache

011 allows a 2-Mbyte E-cache, the largest supported by UltraSPARC-IIi

Behavior for other encodings is Reserved.

PCON[7:0]: Unused on UltraSPARC-IIi; Read as 0

MID[4:0]: Module (processor) ID register; Read as 0

PCAP[16:0]: Read as 0 on UltraSPARC-IIi

Resets are described more fully in Section 17.

