



Sun EDA Compute Ranch



Sun's UltraSPARC Design Team Leverages Dedicated Electronic Design Automation (EDA) Compute Ranch to Deliver Leading Edge Processors.

Leading-edge UltraSPARC processor designs continue to be a critical component of Sun's Intellectual Property portfolio, which is responsible for propelling the company to a leadership role in open standards network computing. As a substantial and highly visible investment in the on-going engineering effort required to create new, incredibly complex "microsystems on a chip," Sun's Compute Ranch (and the world-class processor design team it supports) provides an indisputable, practical demonstration of Sun's unshakable commitment to its UltraSPARC processor line, as well as of its unwavering determination to create entirely new types of highly sophisticated radical Chip MultiThreaded (CMT) designs (like the UltraSPARC T1 or "Niagara" processor) that will blaze the way for computing into the 2nd decade of the 21st century.

Compute Ranch Snapshot: 11/2005

- Accessed by a design team of over 1,000 engineers.
- 3 Design Centers (Sunnyvale, CA; Austin, TX; Burlington, MA).
- Almost 20,000 square feet in combined facilities.
- 15 Years of experience in distributed Grid Computing.
- 95-98% compute utilization (24x7x365).
- Multiple High Availability (HA) clusters delivering FIVE 9s (99.999%) of uptime
- An average of 233,000 jobs/day.
- Close to 3,000 SPARC/Solaris systems.
- Over 10,000 total UltraSPARC processors with an average speed of approximately 1 GHz
- Above 10 trillion compute cycles a second; near a quintillion cycles daily.
- 36 terabytes of RAM.
- Approaching 1.5 petabytes of disk storage.
- 250 EDA tools supported (both commercial and internal)

Compute Ranch Overview

Sun's unparalleled, all SPARC/Solaris™ Compute Ranch exists for one reason only: to apply massive computing power to SPARC processor development. More specifically, the Compute Ranch is a critical aid to Sun's processor engineering team in their quest to achieve the following three primary goals:

- 1) Build into next-generation UltraSPARC processors features and performance unmatched by any competitor.
- 2) Accelerate time-to-market of new UltraSPARC processor products.
- 3) Deliver UltraSPARC processors into production that offer customers best-in-class quality, reliability and uptime.

The Compute Ranch is distributed across three sites: Austin, TX; Sunnyvale, CA; and Burlington, MA. The thousands of machines collectively located at these sites perform countless calculations daily, enabling timely, parallel design, simulation and verification of multiple chips, each integrating hundreds of millions of transistors. For example, at the same time trillions of cycles were being spent to help verify the 300M transistor UltraSPARC IV design, far more cycles were being spent to support concurrent work on the 300M transistor UltraSPARC T1 design together with the (much higher transistor count) future generation "Niagara 2" and "Rock" designs.

Complexity Increases Exponentially

Since 1987, when Sun released its first system based on SPARC® (Scalable Processor ARChitecture) technology, the relentless, exponential growth in the number of transistors per chip (which doubles every two years, in accord with "Moore's Law") has multiplied the issue of design complexity by many thousands of times. Thus, while the initial generation of SPARC processors was implemented using fewer than 100,000 transistors, by 1990 Sun's design team had begun work on a new superscalar generation of SPARC processors, requiring more than 3M transistors to implement (SuperSPARC II).

Confronted by this burgeoning explosion in transistor counts, SPARC engineers envisioned a way to dramatically change the way in which next-generation processors are created, enabling the ever-increasing complexity of chip design to be managed both at the physical and project management levels, while still reaching strict product quality and performance goals. The Compute Ranch is a major part of that solution. First, it brings massive processing power to bear on the task of chip design. Second, it provides an environment in which the overall design process can be managed efficiently, greatly boosting the productivity of Sun's large and technically demanding SPARC design team.

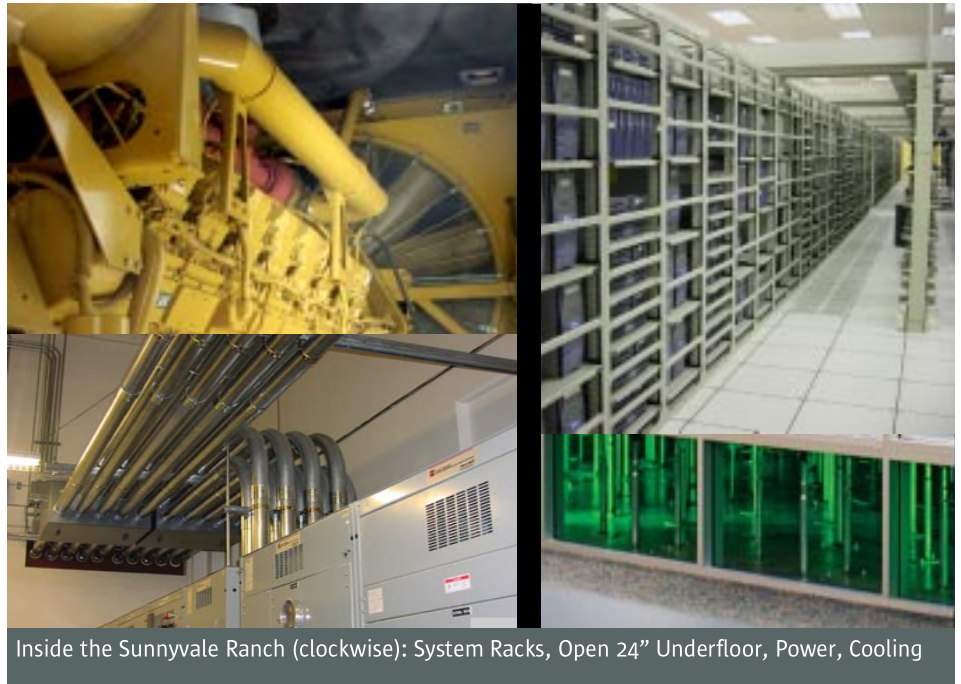
The Compute Ranch for Maximum Efficiency

The initial Ranch vision of the early 1990s has developed today into the most advanced, processor design computing infrastructure on the planet. Between its three locations, Sun's Compute Ranch encompasses nearly 20,000 square feet of space, virtually uniting about 3000 Sun systems that incorporate more than 10,000 UltraSPARC processors, about 36 terabytes of RAM, and nearly 1.5 petabytes of disk storage. This vast distributed compute resource is shared by over 1,000 Sun chip designers, running 250 EDA tools (both commercial and internally developed).

A Distributed, Balanced Managed Resource

To maximize productivity, Ranch management software accepts tens of thousands of job requests daily from Sun's designers, and distributes these workloads across the 3 widely separated Ranch sites. The result is a single, virtual facility that can move workloads freely between both sites and servers to balance utilization, deliver maximum efficiency, and manage numerous design projects simultaneously. The bottom line is a highly flexible, extremely efficient Compute Ranch, achieving up to 98% utilization, while operating around the clock on a 24 x 7 x 365 basis.

The server infrastructure is 100% "Sun-on-Sun": i.e., every single system is based on SPARC processors, runs the Solaris Operating System, and uses Sun StorEdge disks. Current active systems range from desktop Sun Ray™ appliances to Sun Blade™ workstations, and from entry-level Sun Fire™ V440 servers up through the latest 24-processor (48-way) E6900 midframe servers. Included in this mix are the latest 1500 MHz UltraSPARC IV+ dual core processors, older 1200 MHz (and slower) UltraSPARC III processors, and even some aging UltraSPARC II processors operating below 500 MHz. All currently supported Solaris operating environments (8, 9, 10) are represented somewhere in this collection of systems. That fact that the same EDA application software load can be (and is)



Inside the Sunnyvale Ranch (clockwise): System Racks, Open 24" Underfloor, Power, Cooling

freely shifted around between such diverse systems is a dramatic testimony to the value of Sun's long-term commitment to binary software compatibility, across both different implementations and separate generations of its SPARC/Solaris systems.

Within the Compute Ranch are multiple High Availability (HA) clusters, using Sun Cluster™ 3.0 Software to achieve FIVE 9s (99.999%) of uptime to support jobs that may require weeks to complete (and must be restarted from the beginning if interrupted). Over 70 HA-clustered file servers, with fail-over capability, provide 100% mirroring to safely and securely store the massive amounts of sensitive data generated by the designers.

Advanced Facility Design

The Sunnyvale facility was designed from the ground up to serve as the heart of the Compute Ranch, with over twice the floor space of the next largest location to accommodate continued growth. Some of its highlights include:

- 24-inch raised floor with airflow system
- 225,000 cubic feet air recirculation every 45 seconds

- Dry-pipe fire suppression system
- One hour, fire rated, full-height walls
- Rack structure with network and console connections
- Dual 2-megawatt generators
- Redundant power distribution system
- 64 tons of UPS (Uninterrupted Power Supply)

Sun Continues Cutting Edge R&D

With an unrelenting focus on building the world's most advanced 64-bit computing platform, Sun is truly committed to the UltraSPARC technology that powers Sun's technically sophisticated RISC/Unix systems. While recognition of past accomplishments of Sun's processor design team (such as Microprocessor Reports' 2001 Best Workstation/Server processor award for UltraSPARC III) are surely a matter of great pride, the focus of the Compute Ranch is and always has been on the future, developing the next-generation processors that will expand the limits of performance, throughput, scalability, reliability, price, and power consumption for new microsystems.